TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM10N06

60V N-Channel MOSFET

TO-252 (DPAK)

Pin Definition:
1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	R_{DSON} (mΩ)	I_D (A)
60	65 @ V_{GS} = 10V	10
	80 @ V_{GS} = 5V	10
	110 @ V_{GS} = 4V	9

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

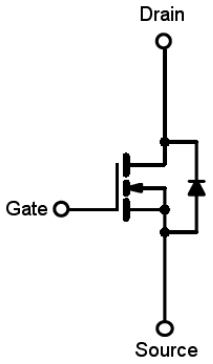
- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM10N06CP ROG	TO-252	2.5Kpcs / 13” Reel

Note: “G” denotes for Halogen Free

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	10	A
Pulsed Drain Current	I_{DM}	50	A
Continuous Source Current (Diode Conduction)[a,b]	I_S	10	A
Total Power Dissipation @ T_C=25°C	P_{DTOT}	45	W
Operating Junction Temperature	T_J	+150	°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JC}$	2.78	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	50	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

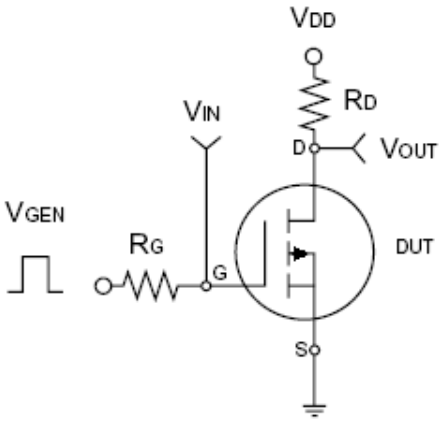
b. Surface Mounted on FR4 Board, t ≤ 10 sec.

TSM10N06
60V N-Channel MOSFET

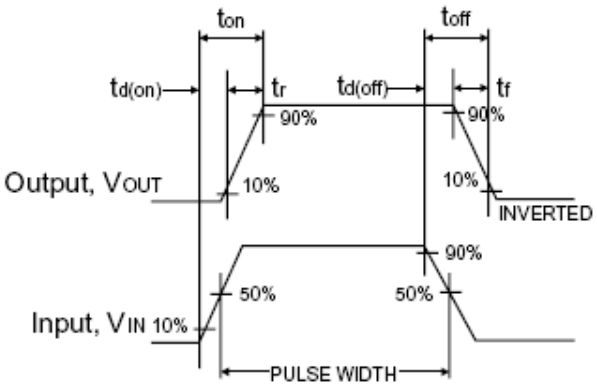
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	1	--	3	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 60V, V_{GS} = 0V	I_{DSS}	--	--	2	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 10A	$R_{DS(ON)}$	--	--	65	mΩ
	V_{GS} = 5V, I_D = 10A		--	--	80	
	V_{GS} = 4V, I_D = 9A		--	--	110	
Forward Transconductance	V_{DS} = 25V, I_D = 6A	g_{fs}	--	13	--	S
Diode Forward Voltage	I_S = 2A, V_{GS} = 0V	V_{SD}	--	0.9	1.2	V
Dynamic[2]						
Total Gate Charge	V_{DS} = 30V, I_D = 9A, V_{GS} = 4.5V	Q_g	--	10.5	16	nC
Gate-Source Charge		Q_{gs}	--	3.5	--	
Gate-Drain Charge		Q_{gd}	--	4.2	--	
Input Capacitance	V_{DS} = 30V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1100	--	pF
Output Capacitance		C_{oss}	--	90	--	
Reverse Transfer Capacitance		C_{rss}	--	55	--	
Switching[2,3]						
Turn-On Delay Time	V_{DD} = 30V, R_L = 5.4Ω, I_D = 9A, V_{GEN} = 10V, R_G = 1Ω	$t_{d(on)}$	--	10	15	nS
Turn-On Rise Time		t_r	--	15	25	
Turn-Off Delay Time		$t_{d(off)}$	--	25	40	
Turn-Off Fall Time		t_f	--	10	15	

Notes 1: Pulse test: PW ≤300μS, duty cycle ≤2%
Notes 2: For DESIGN AID ONLY, not subject to production testing.
Notes 3: Switching time is essentially independent of operating temperature.



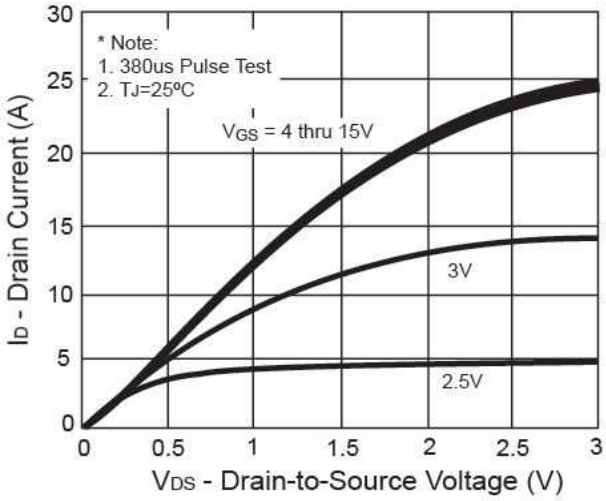
Switching Test Circuit



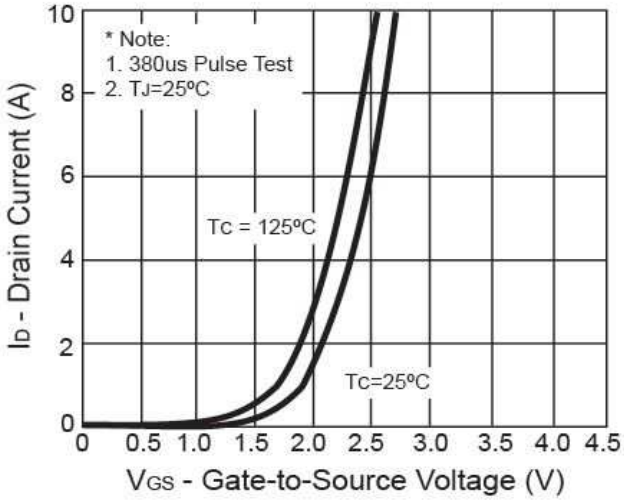
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

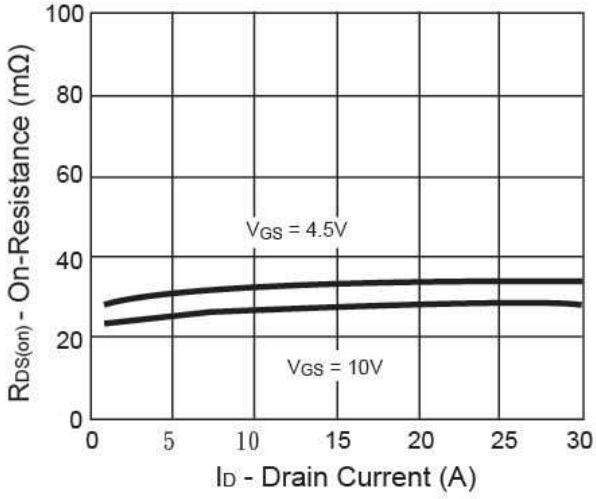
Output Characteristics



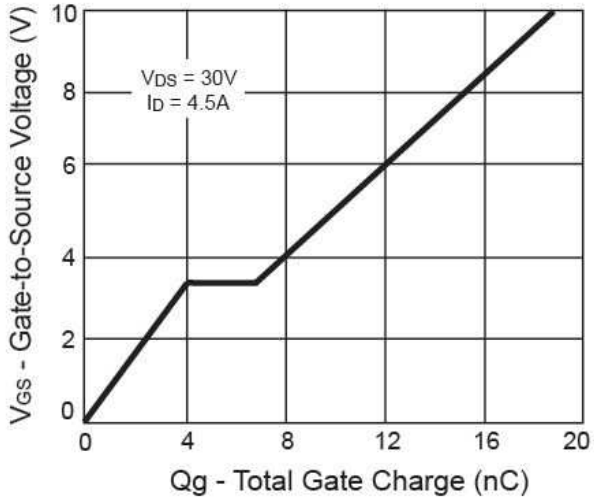
Transfer Characteristics



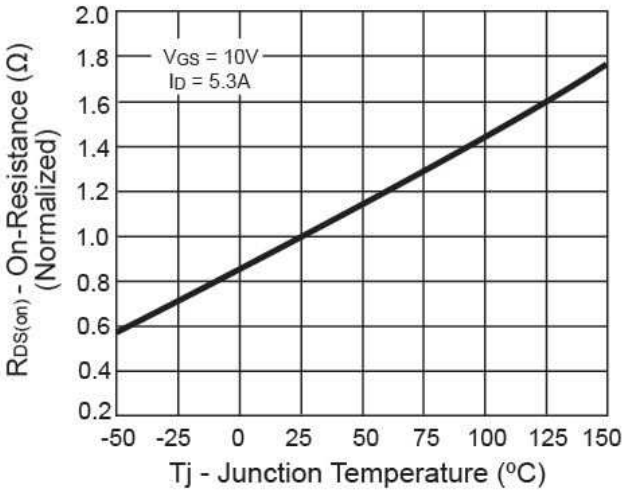
On-Resistance vs. Drain Current



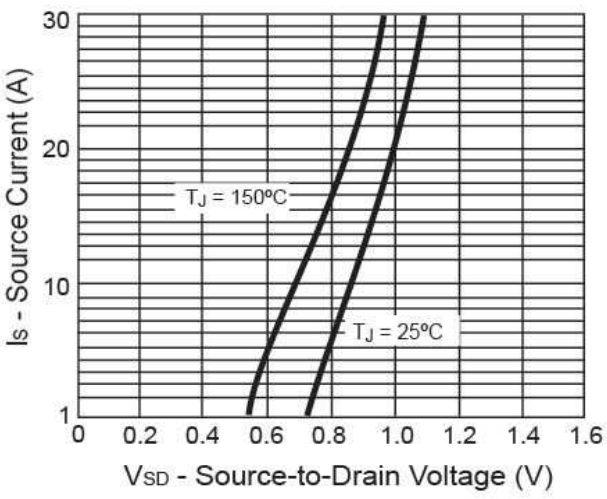
Gate Charge



On-Resistance vs. Junction Temperature

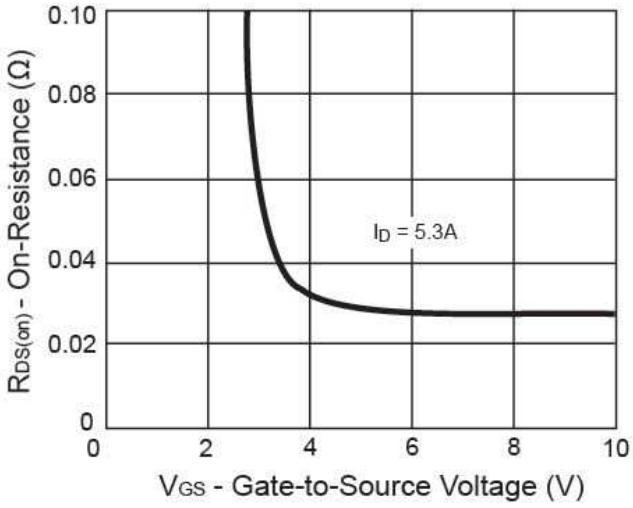


Source-Drain Diode Forward Voltage

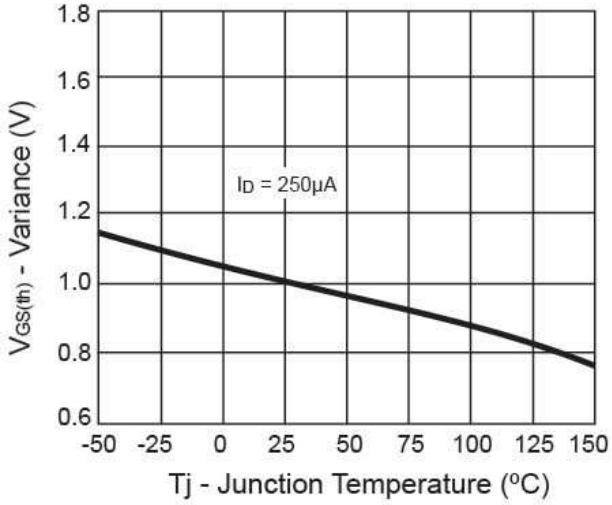


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

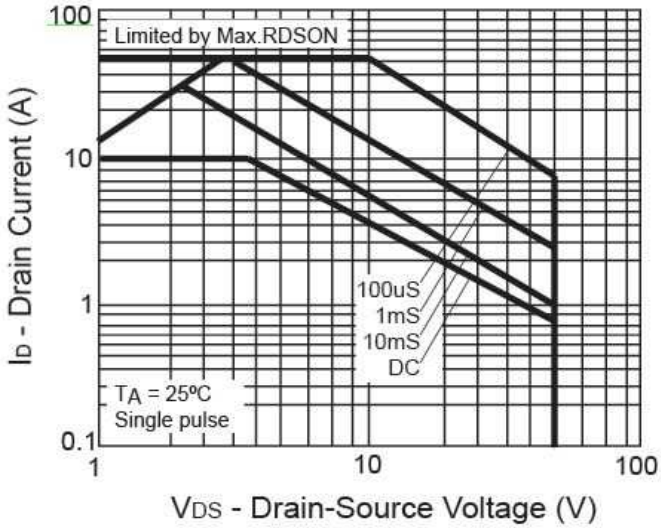
On-Resistance vs. Gate-Source Voltage



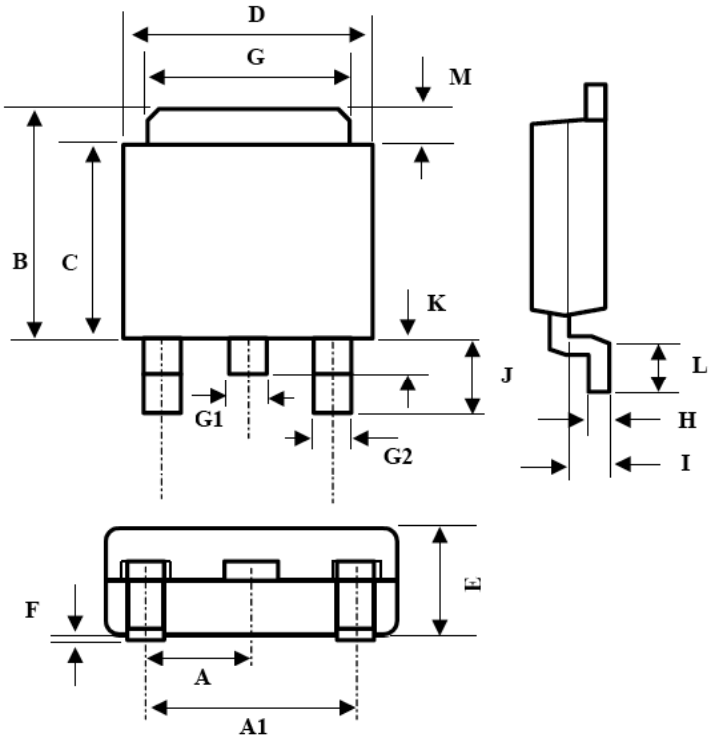
Threshold Voltage



Maximum Safe Operating Area



TO-252 Mechanical Drawing



TO-252 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.3BSC		0.09BSC	
A1	4.6BSC		0.18BSC	
B	6.80	7.20	0.268	0.283
C	5.40	5.60	0.213	0.220
D	6.40	6.65	0.252	0.262
E	2.20	2.40	0.087	0.094
F	0.00	0.20	0.000	0.008
G	5.20	5.40	0.205	0.213
G1	0.61	0.78	0.024	0.030
G2	0.51	0.71	0.020	0.028
H	0.35	0.65	0.014	0.026
I	0.90	1.50	0.035	0.059
J	2.20	2.80	0.087	0.110
K	0.50	1.10	0.020	0.043
L	0.90	1.50	0.035	0.059
M	1.30	1.70	0.051	0.67

Marking Diagram

Y = Year Code
M = Month Code for Halogen Free Product

O =Jan	**P** =Feb	**Q** =Mar	**R** =Apr
S =May	**T** =Jun	**U** =Jul	**V** =Aug
W =Sep	**X** =Oct	**Y** =Nov	**Z** =Dec

L = Lot Code

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