TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM3404

30V N-Channel MOSFET

SOT-23

Pin Definition:
1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
30	30 @ V_{GS} = 10V	5.8
	43 @ V_{GS} = 4.5V	5.0

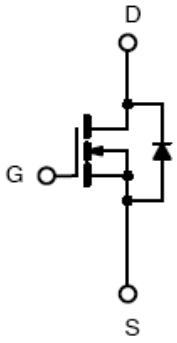
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM3404CX RF	SOT-23	3Kpcs / 7" Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current		I_D	5.8	A
Pulsed Drain Current		I_{DM}	20	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	2.5	A
Maximum Power Dissipation	Ta = 25°C	P_D	0.75	W
	Ta = 75°C		0.48	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Foot Thermal Resistance	$R\Theta_{JF}$	75	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	140	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 10 sec.

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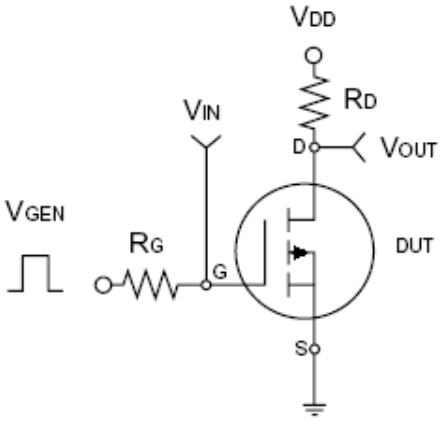
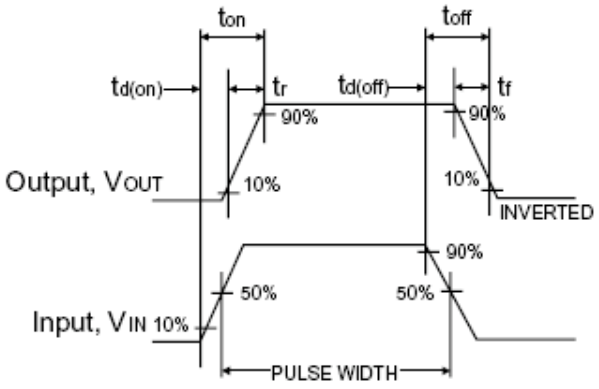
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	30	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	1	1.4	3	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	μA
Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V	I_{DSS}	--	--	1.0	μA
On-State Drain Current	V_{DS} = 5V, V_{GS} = 4.5V	$I_{D(ON)}$	20	--	--	A
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 5.8A	$R_{DS(ON)}$	--	23	30	mΩ
	V_{GS} = 4.5V, I_D = 5A		--	35	43	
Forward Transconductance	V_{DS} = 5V, I_D = 5A	g_{fs}	--	25	--	S
Diode Forward Voltage	I_S = 1.0A, V_{GS} = 0V	V_{SD}	--	0.76	1	V
Dynamic[b]						
Total Gate Charge	V_{DS} = 15V, I_D = 5.8A, V_{GS} = 10V	Q_g	--	4.52	--	nC
Gate-Source Charge		Q_{gs}	--	1.24	--	
Gate-Drain Charge		Q_{gd}	--	1.68	--	
Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	400.96	--	pF
Output Capacitance		C_{oss}	--	100.47	--	
Reverse Transfer Capacitance		C_{rss}	--	71.82	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = 15V, R_L = 2.2Ω, I_D = 1A, V_{GEN} = 10V, R_G = 6Ω	$t_{d(on)}$	--	7.42	--	nS
Turn-On Rise Time		t_r	--	3.41	--	
Turn-Off Delay Time		$t_{d(off)}$	--	20.4	--	
Turn-Off Fall Time		t_f	--	3.01	--	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



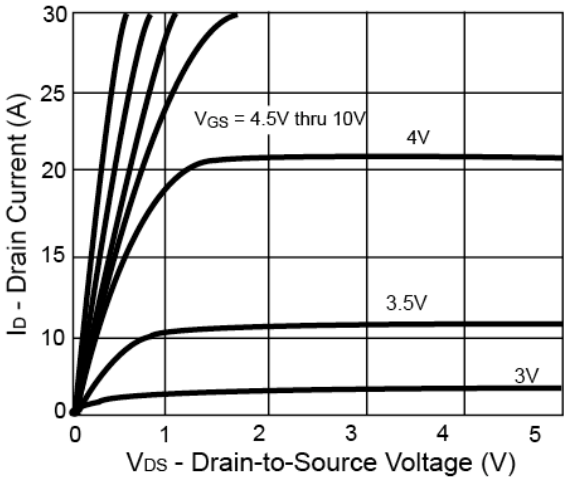
Switching Test Circuit



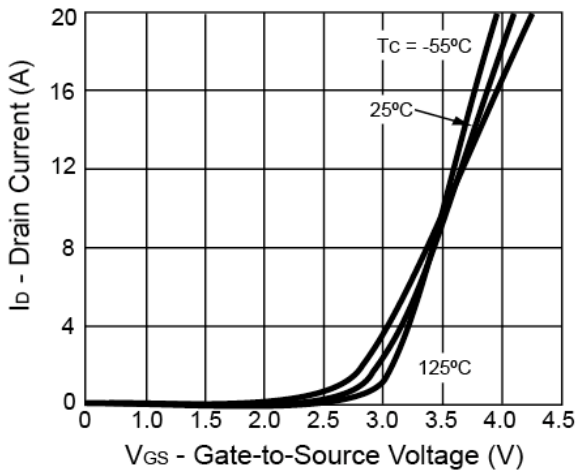
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

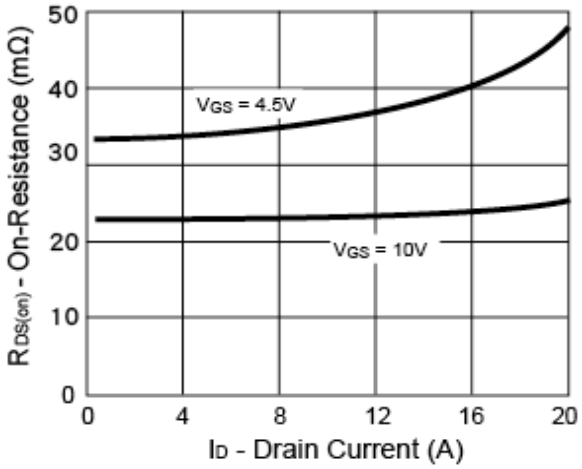
Output Characteristics



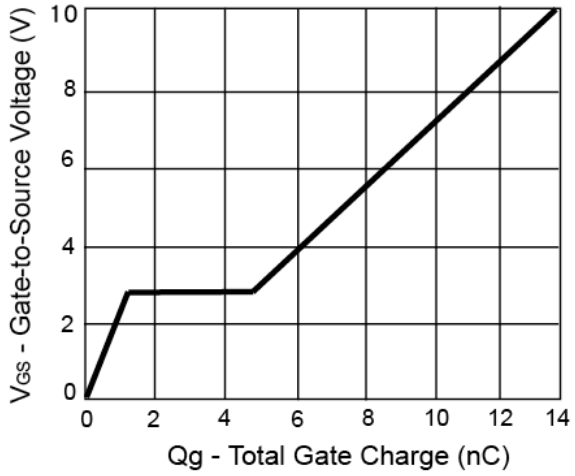
Transfer Characteristics



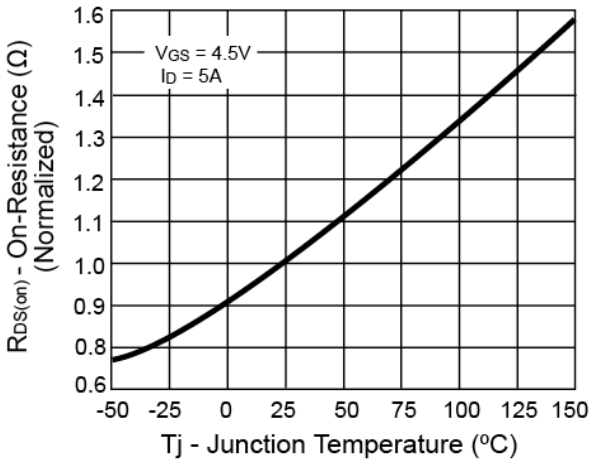
On-Resistance vs. Drain Current



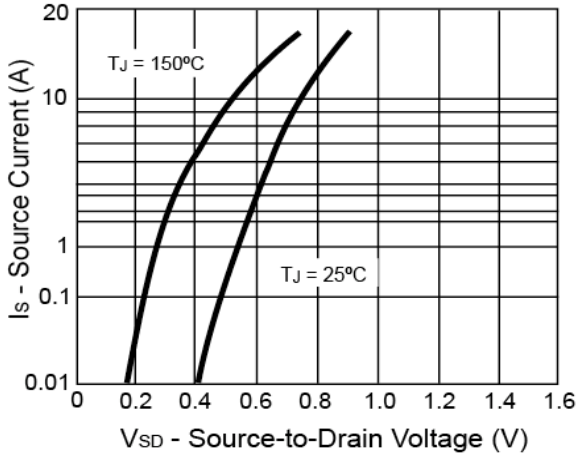
Gate Charge



On-Resistance vs. Junction Temperature

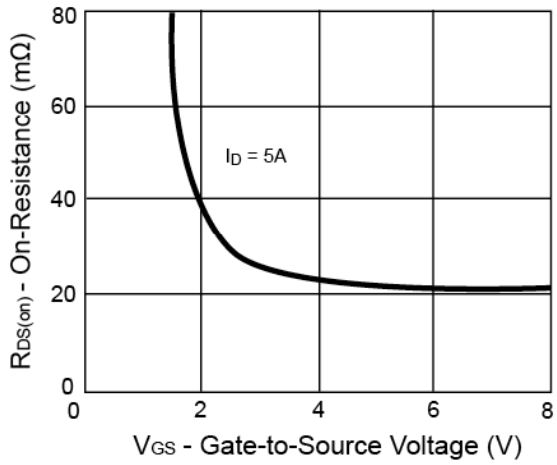


Source-Drain Diode Forward Voltage

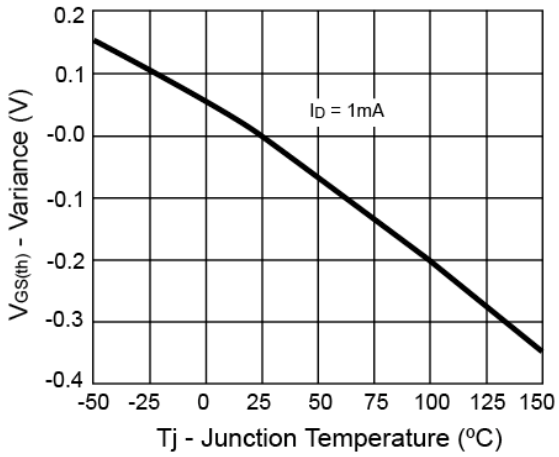


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

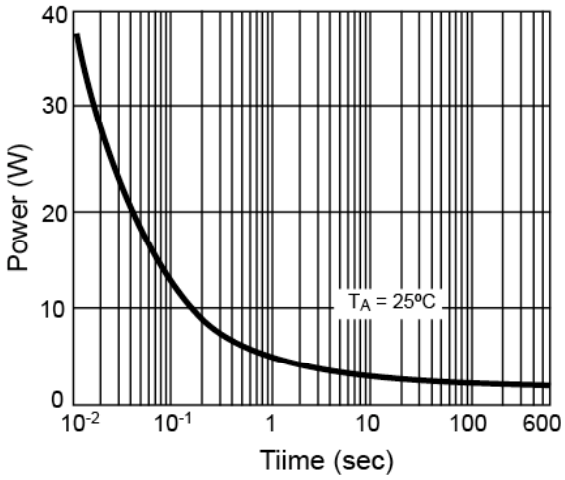
On-Resistance vs. Gate-Source Voltage



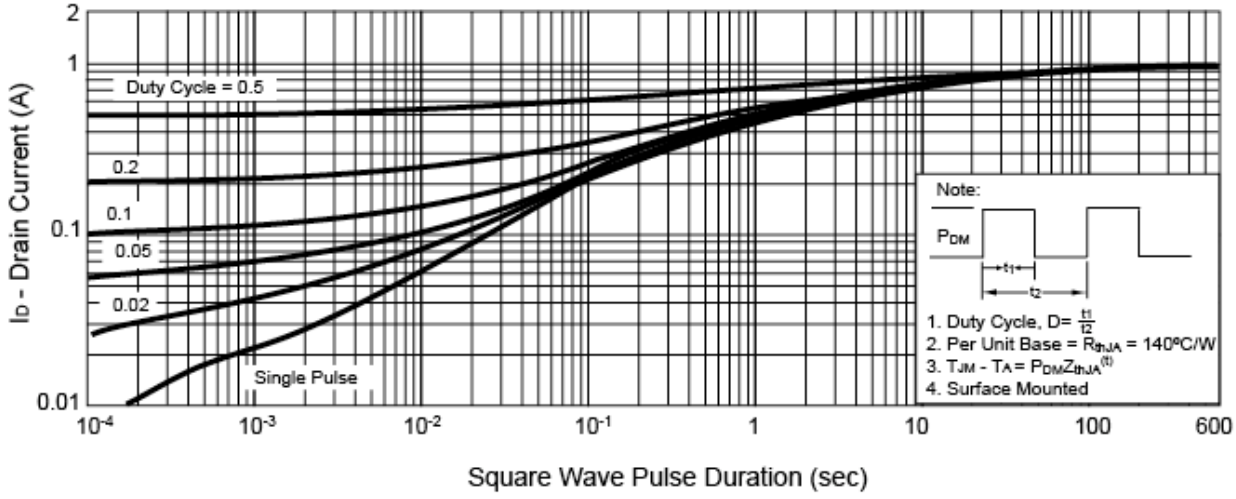
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



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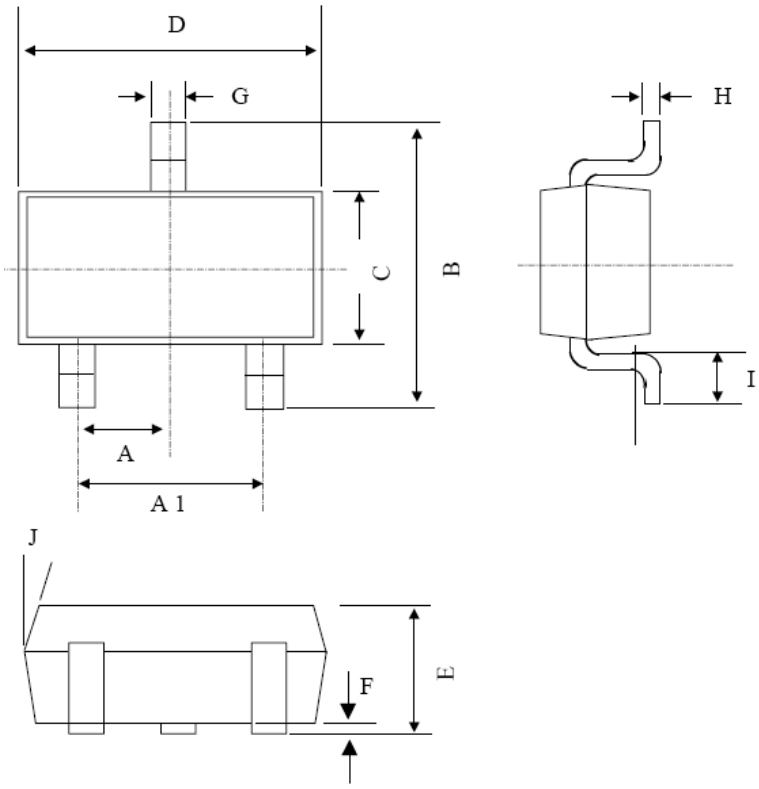
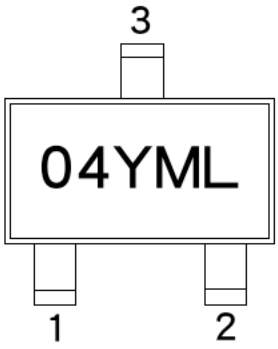
SOT-23 Mechanical Drawing



SOT-23 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	0.95 BSC		0.037 BSC	
A1	1.9 BSC		0.074 BSC	
B	2.60	3.00	0.102	0.118
C	1.40	1.70	0.055	0.067
D	2.80	3.10	0.110	0.122
E	1.00	1.30	0.039	0.051
F	0.00	0.10	0.000	0.004
G	0.35	0.50	0.014	0.020
H	0.10	0.20	0.004	0.008
I	0.30	0.60	0.012	0.024
J	5°	10°	5°	10°

Marking Diagram



04 = Device Code
Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
L = Lot Code

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